A Hierarchical Graph Neural Network-Based Methodology for SRAM Cell-Aware Model Generation

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ABSTRACT

Testing and diagnosing embedded memories is critical to ensure SoC quality and reliability, and to accelerate yield ramp-up, especially in safety-critical domains such as automotive and defense. As technology nodes continue to shrink, memories become increasingly vulnerable to manufacturing defects, while the cost and complexity of their validation and diagnosis keep rising. Cell-Aware (CA) model generation aims at characterizing intra-cell defects at the transistor level. However, the current state of practice still relies heavily on exhaustive analog SPICE defect simulation, which is time-consuming and complex in the context of dense memory circuits. Machine learning-based (ML-based) approaches have already been proposed to accelerate CA model generation for standard cells. The latest method uses a Random Forest algorithm to predict defect behavior, coupled with a decision block based on ML that selects, for each (defect, stimuli) pair, whether to rely on the machine learning model or to fall back to SPICE simulation, thereby accelerating the generation of CA models for standard cell libraries independently of the technology. Building on this concept, we aim to minimize, and possibly eliminate, the use of analog simulations for CA model generation in SRAMs by exploiting the structural hierarchy of their circuitry through graph-based learning. We propose a hierarchical GNN-based approach in which the SRAM circuitry is decomposed into several hierarchical levels (compartment, primary block, module, and top level), and a graph neural network is used to predict the CA model at each level, following a bottom-up approach. The CA model obtained at level $(n-1)$ would then be treated as a black-box component to construct an abstracted graph, which would subsequently be used by the GNN to generate the CA model at level (n), thus enabling scalable and efficient CA modeling of realistic SRAM architectures.

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